REMARKS

Claims 1-14 are pending in the application. The Examiner's reconsideration of the objection and rejections in view of the amendments and remarks is respectfully requested.

Applicant appreciates the Examiner's indication that claims 6-14 are allowed and that claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 1 and 3-5 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Christiansen, U.S. Patent No. 5,961,614, in view of applicant's admitted prior art. The Examiner stated essentially that Christiansen and admitted prior art teach or suggest all the limitations recited in claims 1 and 3-5.

Claim 1 claims, *inter alia*, "a direct memory access (DMA) controller which determines the flag bit allotted by the central processing unit, and according to the flag bit, stops processing a buffer descriptor currently being accessed and accesses a next buffer descriptor, or processes packet data according to information stored in the buffer descriptor currently being accessed."

Christiansen teaches that when the Ethernet controller determines that data packet transmission to the I/O controller has been completed, the Ethernet controller sets the status register to indicate the status of the packet that was just transmitted and generates an interrupt signal as a status bit (see col. 5, lines 59-64 and Figure 8, S2'). Christiansen teaches that the device may not proceed to send a status bit unit a transmission has been complete (see Figure 8). Christiansen does not teach that, according to the flag bit, a DMA stops processing a buffer

descriptor currently being accessed and accesses a next buffer descriptor, essentially as claimed in claim 1. Nowhere does Christiansen teach or suggest that a DMA stops a current process and begins a next process. Christiansen teaches that a transmission of a data packet continues until complete (see Figure 8, S1' and S2'). Christiansen does not teach or suggest stopping processing of a buffer descriptor currently being accessed and accessing a next buffer descriptor, essentially as claimed in claim 1. Therefore, Christiansen fails to teach or suggest all the limitations of claim 1.

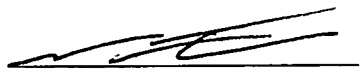
The Description of Related Art teaches "a communication system that transmits/receives packet data via two or more communication channels, if an error occurs in one of the communication channels, and thus the DMA controller is in a standby mode, the DMA controller cannot process packet data transmitted via error-free communication channels." Clearly, the Description of Related Art does not teach or suggest "a direct memory access (DMA) controller which... stops processing a buffer descriptor currently being accessed and accesses a next buffer descriptor", as claimed in claim 1.

The combined teachings of Christiansen and the Description of Related Art do not teach or suggest "a direct memory access (DMA) controller which... stops processing a buffer descriptor currently being accessed and accesses a next buffer descriptor" as claimed in claim 1. The Examiner's reconsideration of the rejection is respectfully requested.

Claims 3-5 depend directly or indirectly from claim 1. The dependent claims are believed to be allowable for at least the reasons given for claim 1. The Examiner's reconsideration of the rejection is respectfully requested.

For the forgoing reasons, the application, including claims 1-14, is believed to be in condition for allowance. Early and favorable reconsideration of the case is respectfully requested.

Respectfully submitted,

By: 

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